ESSTMAGS Product Datasheet

Magnetic rotary absolute position encoder

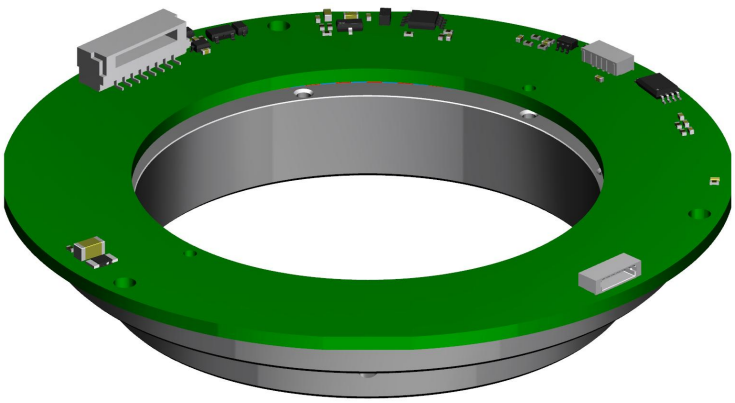
Product series: EAS-017

Product part number: EAS-017-A

EAS-017-D

Version: Ver1.0.5

Date: 2026-07-10



CONTENTS

1. Description

EAS series product is an absolute linear position detection magnetic encoder. The sensor can be used in a movement control system to detect the position, speed of the system.

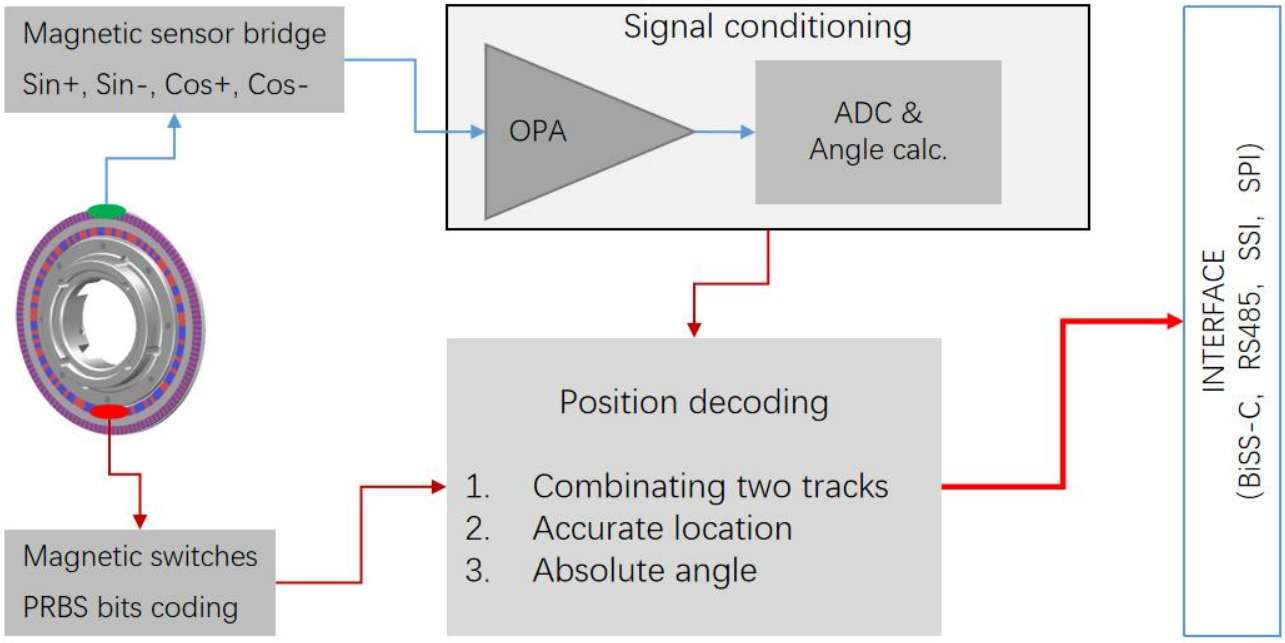
The sensor uses non-contact detection method based on TMR magnetic sensing technology. The magnetic scale has two magnetic tracks (incremental and absolute tracks).

The sensor has build-in signal processing circuit, and a digital output of RS485 format.

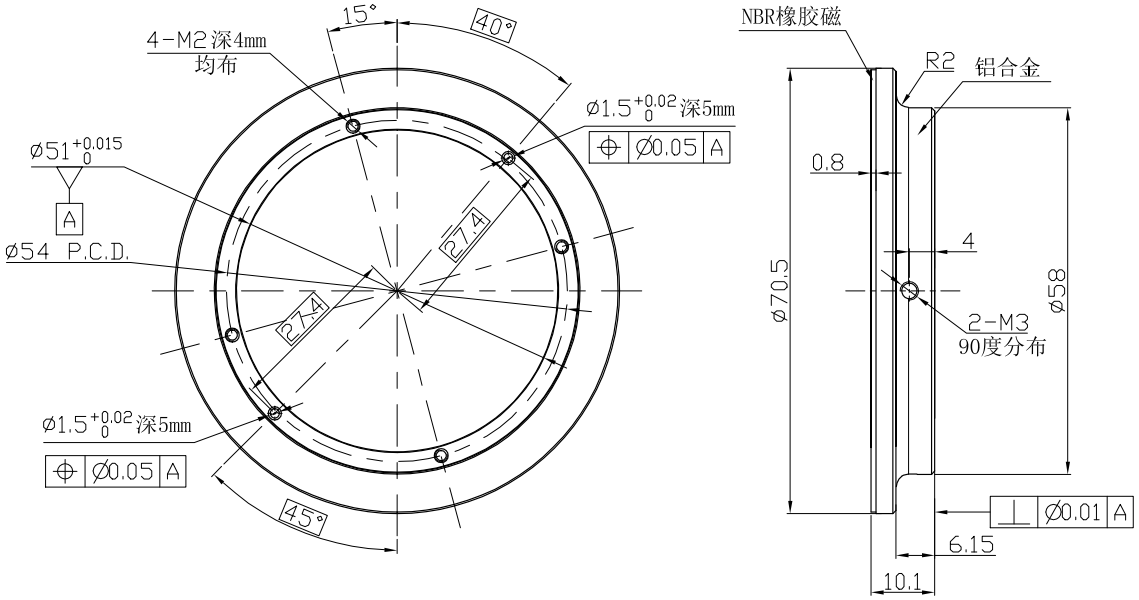
EAS series product has the following features:

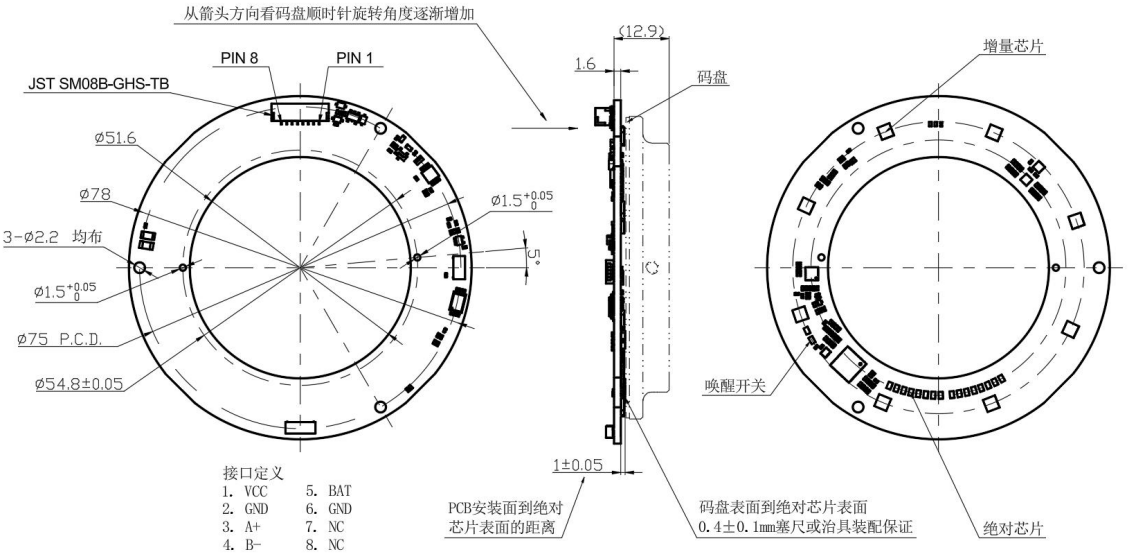
- True absolute value system
- Absolute position dual track system
- Customized sensor chips
- The system is self-calibrating
- Single-turn resolution 23 bits, multi-turn resolution 16 bits
- The repeatability is 5 arc seconds
- Absolute positioning accuracy 10 arcseconds
- RS485, BISS interface

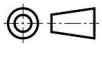
2. Product part number



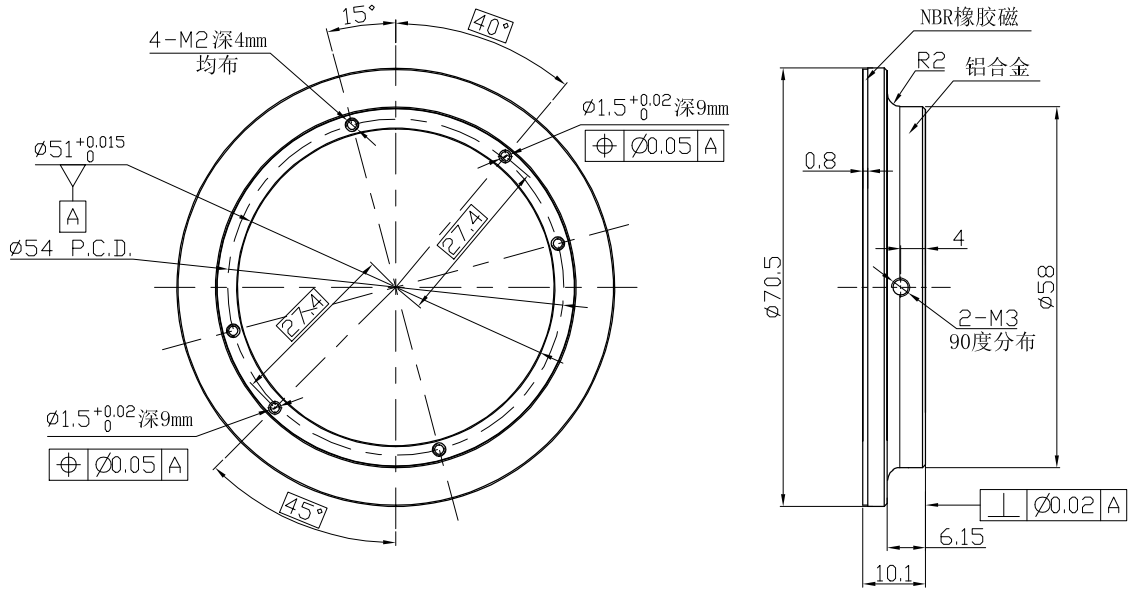
3. EAS-017-A Dimensions

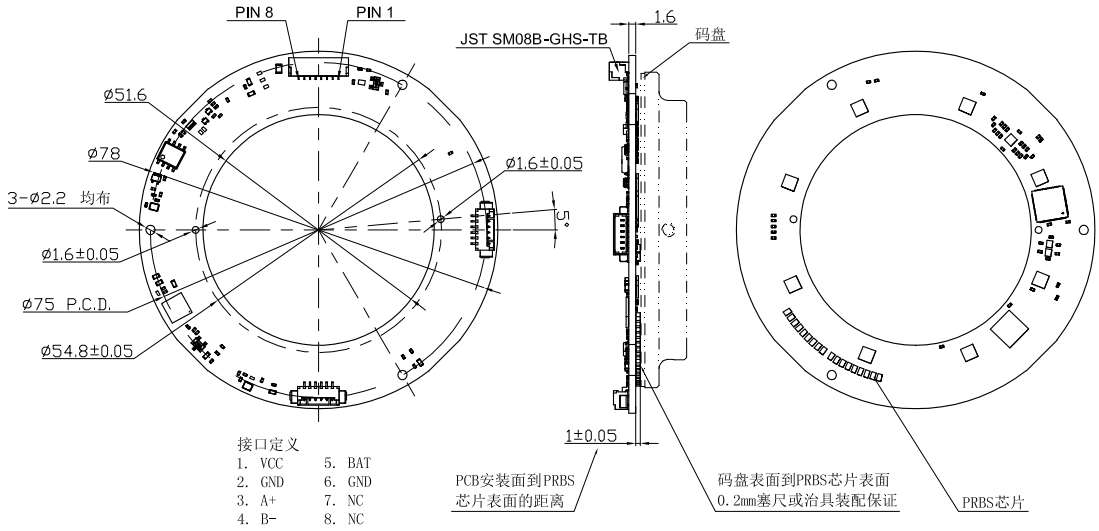


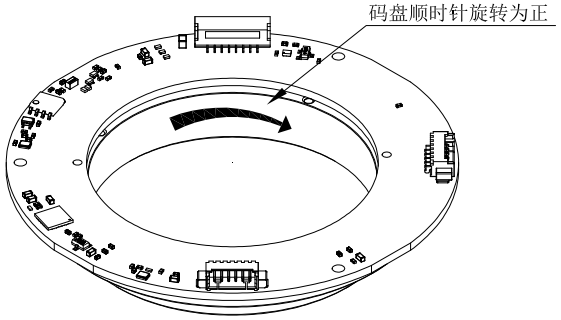




4. EAS-017-D Dimensions







5. Electrical characteristic

5.1. EAS-017-A Electrical connection

Lead	NAME
1	VCC
2	GND
3	A+
4	B-
5	BAT
6	GND
7	NC
8	NC

5.2. EAS-017-D Electrical connection

Lead	NAME
1	VCC
2	GND
3	CLK-
4	CLK+
5	DATA-
6	DATA+
7	BAT
8	Reset

5.3. General parameter

Operating and storage temperature	–40℃ to +105℃ (Note: The operating temperature of the diode on the encoder is -40℃ to +85℃)
Humanity	70%Rh
External magnetic field (thickness direction)	±100 mT
Shock (dependent on installation)	100 g
Vibration (dependent on installation)	80 g

5.4. Environmental parameter

Supply voltage	4.75V~5.25V
Current	100 mA~150 mA
Connector	8-pin
Start-up time	100 ms
ESD (HBM)	HBM, Class 2, ±2 kV

5.5. System parameter

Parameter	Unit	Min	Typ	Max	Comment
Resolution	bit		20		One lap
			16		Loopy
Maximum speed	RPM		10000		
Repeatability	arcsec		±5		Bidirectional 3 cycles
Absolute position error	arcsec		±10		
Input bandwidth	kHz			18	
Noise	°		±0.0005		

6. RS485 protocol interface

6.1 Summarize

Item	Description	Remark
Transmission type	Differential drive	RS485
Receiving type	Differential drive	RS485
Transmission data	Single turn data	24bits
Communication rate	2.5Mbps	

6.2 Communication interface

Communication parameter	
Baud rate	2.5M
Baud rate	8bits
Parity check	NC
Stop bit	1
Flow control	NC
Request communication mode	Passive corresponding communication

6.3 Frame format

Request	Control field												
	CM												
Transmission data from		<5 μs	Control	Status	Data field								CRC field
			CM	SA	D0	D1	D2	D3	D4	D5	D6	D7	CRC

6.4 Details

6.4.1 Control field (CM)

The following table shows the structure of the control domain.

Start bit	Sink code			Data ID code				ID parity	Delimiter
0	0	1	0	dc0	dc1	dc2	dc3	dc4	1

(1) Start bit: fixed.

(2) Sink code: Fixed.
(3) Data ID code: See Table 6-4-1.
(4) ID parity: This is the parity of the data ID code.
(5) Separator: fixed.

Table 6-4-1 Data ID code table

Application	Data ID	Code				Parity
		dc0	dc1	dc2	dc3	dc4
Readout of data	Data ID 0 (0x02)	0	0	0	0	0
	Data ID 1 (0x8A)	1	0	0	0	1
	Data ID 2 (0x92)	0	1	0	0	1
	Data ID 3 (0x1A)	1	1	0	0	0
Writing to EEPROM	Data ID 6 (0x32)	0	1	1	0	0
Readout from EEPROM	Data ID D (0xEA)	1	0	1	1	1
Reset	Data ID7 (0xBA)	1	1	1	0	1
	Data ID 8 (0xC2)	0	0	0	1	1
	Data ID C (0x62)	0	0	1	1	0

6.4.2 State Area (SA)

The state domain structure is shown in Table 6-4-2。

Table 6-4-2 state domain structure

Start bit	Information				Encoder error		Communication alarm		Delimiter
0	sd0	sd1	sd2	sd3	er0	er1	cl0	cl1	1

(1) Start bit: fixed.

(2) Information: All fixed as "0".
(3) Encoder error: sends logic "1" when any error occurs in the encoder.

6.4.3 Data field

The relationship between data ID codes and data fields is shown in Table 6-4-3.

Table 6-4-3 Lists the data domains

Data ID code	D0	D1	D2	D3	D4	D5	D6	D7
Data ID 0 (0x02)	AS0	AS1	AS2					

Note: The blank in the table above indicates the number not transmitted

6.4.4 CRC Verification Domain (CRC)

Table 6-4-4 shows the CRC domain structure.

Table 6-4-4 CRC domain structure

Start bit	CRC code(LSB first)								Delimiter
0	cr0	cr1	cr2	cr3	cr4	cr5	cr6	cr7	1

(1) Start bit: fixed.
(2) CRC check code: This code conforms to the equation G(X) = X8 + 1 (X = cr0~cr7). The data is first arranged by LSB. The code is calculated based on all bits of all fields except CRC fields, excluding the start bit and separator.
(3) Separator: fixed.

6.4.5 Structure of Detailed status bits

Detailed status	
bit12	flash_crc_error
bit13	magic_error
bit14	temp_alarm
bit15	chip_fflt
bit16	prbs_error

6.4.6 Transmit and receive interface circuit diagram

An example of the transmit and receive interface circuit diagram is shown in Figure 6-4-5.

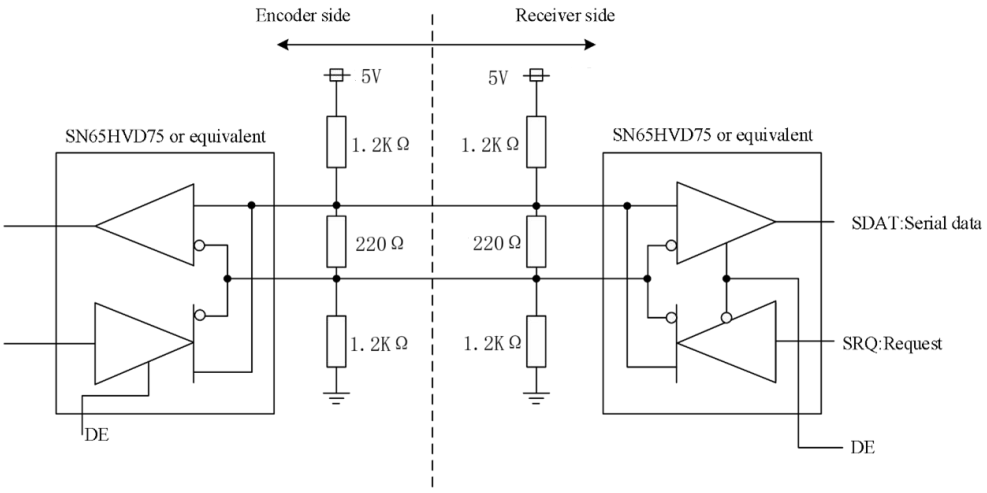


Figure 6-4-5 Example of transmit and receive interface circuits

When the encoder transmits data, do not send any requests to the encoder. If any requests are sent to the encoder in error during this period, the encoder's interface circuit may be interrupted. In addition to transmitting data, the encoder is always in receive mode.

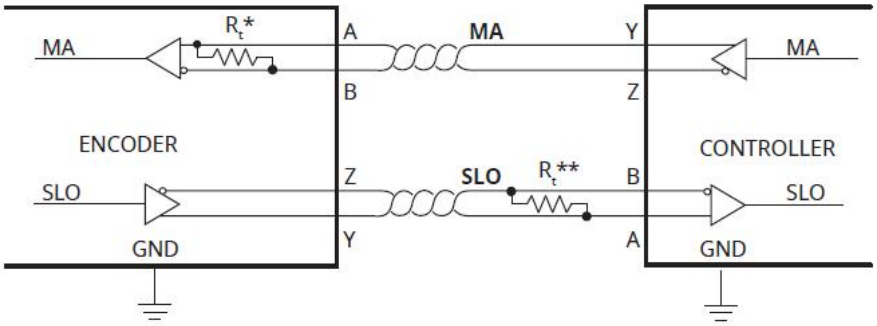
7. BISS protocol interface

8. Clock frequency	400 kHz ~ 2.5 MHz
Maximum request rate	44 kHz
Resolution	24Bit
Delay	<10 μs

BISS protocol interface:

The encoder position is represented using a 24-bit natural binary code, and the encoder status is available via the BiSS C protocol. The position data is aligned to the left. Following the position data are two status bits (active low), and then the CRC (inverted).

Electrical connection



Signal	
MA	Master clock, the maximum clock frequency is 2.5Mhz
SLO	The data is output on the rising edge of the MA

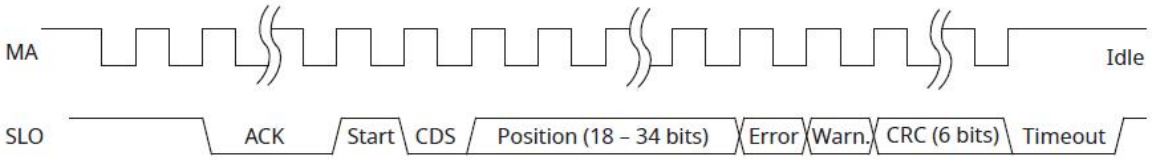
* The MA and SLO lines are 5V RS422 compatible differential pairs. The termination resistor on the MA line is integrated inside the encoder.

** If the total cable length is more than 5 meters, it needs to be terminated at the controller. The cable has a nominal impedance of 120Ω.

Output protection

Two mechanisms prevent excessive output current and power loss due to errors or bus collisions. Reverse current limiting on the output stage provides immediate protection against short circuits. In addition, if the chip temperature is too high, the thermal shutdown circuit forces the driver output into a high-impedance state.

BiSS C timing diagram

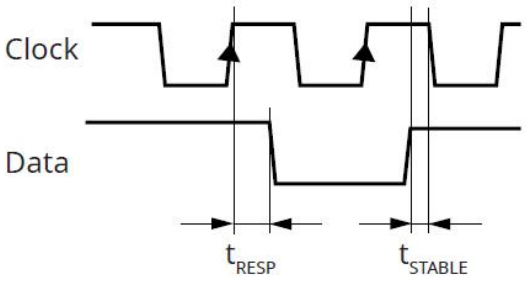


The MA is in a high state and communication starts at the first falling edge.
The encoder sets the SLO low at the second rising edge of the MA, and the ACK length is 1~30 bits.
When the encoder is ready for the next request cycle, it indicates this to the host by setting the SLO to high.
Absolute position and CRC data are provided in binary format and are first sent in MSB format.

Cable length compensation

The read head takes 170 ns to respond to the incoming clock (tRESP). The change in the data signal is delayed by 170 ns after the rising edge of the clock line. The additional delay is caused by the time it takes for the signal to propagate through the cable to the read head and back (tPROP). This delay is typically 14ns per 14 meters of cable. The total cable length from the encoder to the receiver must be considered.

$$t_{DELAY} = t_{RESP} + t_{PROP} \times \text{cable length}$$



Before a value can be latched, the data signal must be stable. Therefore, if the cable length is more than 1 meter and the clock frequency is higher than 1MHz, this delay must be compensated in the receiver (controller) to which the encoder is connected.

Status bits

type	Value 0	Value 1	Description
Error	Location data is invalid	OK	Error bit activation is low. If it is low, the bit is invalid
Warn	Location data is valid	OK	The warning bit is active low. If it is low, the encoder operation is close to its limit. The location is still valid, but the resolution and/or accuracy may be out of specification

Communication parameters

The communication interface variant in the product model defines the functions of the encoder.

Communication interfaces	Parameter	Value
C	MA frequency	Max. 2.5 MHz
	ACK length	1~30 bit
	Register access	no

*The "Bandwidth" parameter is the mechanical bandwidth. AksIM samples at 18 kHz, so the mechanical change occurs faster than 9 kHz and the output cannot be detected (Nyquist's theorem). If the position request is faster than the sampling frequency, the AksIM encoder recalculates the position at the time of the request based on the current ring velocity.

Packet description

24-bit position + 2-bit status + 6-bit CRC = 32-bit long packets.

The CRC calculation polynomial for position, error, and warning data is: x6 + x1 + 1. It is also denoted as 0x43. It is inverted and transmits the MSB first.